

REMARKS

Claims 1-18 are pending in this application. By this Amendment, claims 1 and 5 are amended. No new matter is added. Support for the amendments to claims 1 and 5 may be found at, for example, Figs. 1, 2, 3C, 4-8 and 12-13, as filed.

I. Rejections Under 35 U.S.C. §103(a)

Claims 1-5, 8, 11, 14, 17 and 18 are rejected under 35 U.S.C. §103(a) over JP 01-164044 (JP 044) in view of U.S. Patent No. 6,445,069 (Ling); and claims 6, 7, 9, 10, 12, 13, 15 and 16 are rejected under 35 U.S.C. §103(a) over JP 044 with Ling as applied to claims 1-5, 8, 11, 14, 17 and 18 and further in view of U.S. Patent No. 6,625,032 (Ito). These rejections are respectfully traversed.

Claim 1 recites an interconnect covering all the lateral surfaces of the metal layer.

Claim 5 recites a step of forming an interconnect as to cover all the lateral surfaces of the metal layer.

These features of claims 1 and 5 are not taught or suggested by JP 044, Ling and Ito, taken in combination or alone. JP 044 merely discloses electrode land portion formed of a single layer of Al or Au. JP 044 fails to disclose, teach or suggest an electrode land portion formed of a plurality of layers as recited in claims 1 and 5.

Ling is relied upon for allegedly teaching a pad formed on a first surface and a metal layer formed of a plurality of layers.

Ito is merely relied upon for allegedly teaching a dispersant ejecting method.

The recitation in claim 1 of an interconnect that covers all the lateral surfaces of the metal layer makes the lateral surfaces less vulnerable in order to improve reliability. This feature, especially, prevents the metal layer from corrosion due to electromigration caused by moisture when a reliability test is carried out in a humid condition. Under such humid conditions, although the metal layer is formed of different material layers, moisture can easily

penetrate between the layers. This feature is clearly illustrated, for example, in Figs. 1 and 2 of the invention, but is not disclosed in the applied references. Claim 5 recites a similar feature in the form of a method claim. Therefore, this benefit is not taught or suggested by the chips, as disclosed by JP 044, Ling or Ito.

For the foregoing reasons, claims 1 and 5, as well as the claims depending therefrom, are not rendered obvious by JP 044, Ling and Ito, taken in combination or alone.

Accordingly, JP 044, Ling and Ito do not suggest claims 1 and 5 or dependent claims 2-4, 8, 11, 14, 17 and 18, which include additional features.

Withdrawal of the rejections is respectfully requested.

II. Double Patenting Rejection

Claims 1-18 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting over claims 1-34 of co-pending U.S. Application No. 10/788,499 in view of JP 044 and Ling. This rejection is respectfully traversed.

U.S. Application No. 10/788,499, JP 044 and Ling each fail to teach or suggest an interconnect covering all the lateral surfaces of the metal layer, as recited in claims 1 and 5 and as discussed above.

For the foregoing reasons, claims 1 and 5, as well as the claims depending therefrom, are not rendered obvious by claims 1-34 of U.S. Application No. 10/788,499 in view of JP 044 and Ling.

Withdrawal of the rejection is respectfully requested.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-18 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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Date: July 7, 2006

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